IN THE CLAIMS:

The following is a complete listing of claims and replaces all prior versions and listings of claims in the present application:

- 1. 25. (Cancelled)
- 26. (Previously Presented) A light-emitting diode arrangement, comprising:
 - a light-emitting diode chip;

a multi-layer board having a base of a thermally well-conducting material, the material including a metal, the base being a core of the board and configured for heat dissipation; and

an electrically insulating and thermally conducting connection layer between an emission surface of the light-emitting diode chip and the board, wherein between the light-emitting diode chip and the base of the board there is arranged an intermediate carrier separate from parts with which the light-emitting diode chip is electrically contacted, and wherein the intermediate carrier includes an aluminum nitride substrate.

27. (Previously Presented) The light-emitting diode arrangement according to claim 26, wherein the electrically insulating connection layer is at least a boundary surface of the light-emitting diode chip, which is arranged towards the board.

- 28. (Previously Presented) The light-emitting diode arrangement according to claim 26, wherein the electrically insulating connection layer is at least an adhesive layer.
- 29. (Previously Presented) The light-emitting diode arrangement according to claim 26, wherein the light-emitting diode chip is accommodated in a depression of the board.
- 30. (Previously Presented) The light-emitting diode arrangement according to claim 26, wherein the light-emitting diode chip is arranged in a region of a depression in the base material of the board.
- 31. (Previously Presented) The light-emitting diode arrangement according to claim 29, wherein the light-emitting diode chip does not project beyond a contour of the board.
- 32. (Previously Presented) The light-emitting diode arrangement according to claim 29, wherein the light-emitting diode chip ends flush with an upper side of the board.

- 33. (Previously Presented) The light-emitting diode arrangement according to claim 29, wherein the depression functions as a reflector.
- 34. (Previously Presented) The light-emitting diode arrangement according to claim 29, wherein the depression includes walls that are at least partially beveled.
- 35. (Previously Presented) The light-emitting diode arrangement according to claim 26, wherein the light-emitting diode chip is arranged so that the substrate of the light-emitting diode is towards the board.
- 36. (Previously Presented) The light-emitting diode arrangement according to claim 35, wherein a substrate of the light-emitting diode chip is of an electrically insulating material.
- 37. (Previously Presented) The light-emitting diode arrangement according to claim 36, wherein the substrate of the light-emitting diode chip is formed of sapphire.
- 38. (Previously Presented) The light-emitting diode arrangement according to claim 26, wherein the light-emitting diode chip is arranged so that a substrate of the light-emitting diode chip is away from the board.

- 39. (Previously Presented) The light-emitting diode arrangement according to claim 26, wherein the light-emitting diode chip is arranged on the intermediate carrier using a conductive adhesive.
- 40. (Previously Presented) The light-emitting diode arrangement according to claim 26, wherein a side of the intermediate carrier towards the board is electrically insulating.
- 41. (Previously Presented) The light-emitting diode arrangement according to claim 40, wherein a region of the intermediate carrier towards the light-emitting diode chip has conductive regions.
- 42. (Previously Presented) The light-emitting diode arrangement according to claim 26, wherein at least a region of the light-emitting diode chip is covered by a Fresnel lens.
- 43. (Previously Presented) The light-emitting diode arrangement according to claim 42, wherein a region between the board and the lens is at least partially filled by a colour conversion material.

- 44. (Previously Presented) The light-emitting diode arrangement according to claim 43, wherein the colour conversion material is arranged above and alongside the light-emitting diode chip.
- 45. (Previously Presented) The light-emitting diode arrangement according to claim 26, wherein the light emitting diode chip is connected to a circuit board using wires, and the circuit board is applied to the board using an insulating layer positioned therebetween.
- 46. (Previously Presented) A light-emitting diode arrangement, comprising:

a light-emitting diode chip,

a multi-layer board having a base of a thermally well-conducting layer, the layer including a metal, the base being a core of the board and configured for heat dissipation; and

an electrically insulating and thermally conducting connection layer between an emission surface of the light-emitting diode chip and the board, wherein between the light-emitting chip and the base of the board there is arranged an intermediate carrier separate from parts with which the light-emitting diode chip is electrically contacted, and wherein a colour conversion material is arranged above and alongside the light-emitting diode chip.

47. (Currently Amended) A light-emitting diode arrangement, comprising:

a light-emitting diode chip;

a multi-layer board having a base of a thermally well-conducting layer, the layer including a metal, the base being a core of the board and configured for heat dissipation; and

an electrically insulating and thermally conducting connection layer between an emission surface of the light-emitting diode chip and the board, wherein between the light-emitting chip and the base of the board there is arranged an intermediate carrier separate from parts with which the light-emitting diode chip is electrically contacted, and wherein the light-emitting diode chip is arranged on the intermediate carrier using a conductive adhesive.

- 48. (New) The light-emitting diode arrangement according to claim 26, wherein there is no electrically conducting layer between the intermediate carrier and the multi-layer board.
- 49. (New) The light-emitting diode arrangement according to claim 46, wherein there is no electrically conducting layer between the intermediate carrier and the multi-layer board.

- 50. (New) The light-emitting diode arrangement according to claim 47, wherein there is no electrically conducting layer between the intermediate carrier and the multi-layer board.
- 51. (New) The light-emitting diode arrangement according to claim 26, wherein the electrically insulating and thermally conducting connection layer is arranged between the intermediate carrier and the base of the board, whereby starting from the base of the board, the electrically insulating and thermally conducting connection layer is arranged above the base of the board, the intermediate carrier is arranged above the electrically insulating and thermally conducting connection layer, and the light emitting diode chip is arranged above the intermediate carrier.
- 52. (New) The light-emitting diode arrangement according to claim 46, wherein the electrically insulating and thermally conducting connection layer is arranged between the intermediate carrier and the base of the board, whereby starting from the base of the board, the electrically insulating and thermally conducting connection layer is arranged above the base of the board, the intermediate carrier is arranged above the electrically insulating and thermally conducting connection layer, and the light emitting diode chip is arranged above the intermediate carrier.
- 53. (New) The light-emitting diode arrangement according to claim 47, wherein the electrically insulating and thermally conducting connection layer is arranged

between the intermediate carrier and the base of the board, whereby starting from the base of the board, the electrically insulating and thermally conducting connection layer is arranged above the base of the board, the intermediate carrier is arranged above the electrically insulating and thermally conducting connection layer, and the light emitting diode chip is arranged above the intermediate carrier.